

Experimental Verification of the Use of Metal Filled Via Hole Fences for Crosstalk Control of Microstrip Lines in LTCC Packages

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Abstract—Coupling between microstrip lines in dense RF packages is a common problem that degrades circuit performance. Prior three-dimensional-finite element method (3-D-FEM) electromagnetic simulations have shown that metal filled via hole fences between two adjacent microstrip lines actually increases coupling between the lines; however, if the top of the via posts are connected by a metal strip, coupling is reduced. In this paper, experimental verification of the 3-D-FEM simulations is demonstrated for commercially fabricated low temperature cofired ceramic (LTCC) packages. In addition, measured attenuation of microstrip lines surrounded by the shielding structures is presented and shows that shielding structures do not change the attenuation characteristics of the line.

Index Terms—Coupling, crosstalk, microstrip, microwave transmission lines.

I. INTRODUCTION

RF SYSTEMS being planned today integrate more functions in smaller packages that must cost less than those currently being used. Although several packaging technologies have been proposed to meet these goals [1]–[5], low temperature cofired ceramic (LTCC) may be the ideal packaging technology. The material used in LTCC has a moderate relative dielectric constant, ϵ_r , between four and eight, which permits wider microwave transmission lines and has lower conductor loss than circuits on Si, GaAs, and Alumina. It also has a low loss tangent of 0.002 at 10 GHz, which results in low dielectric attenuation. Packages are built with multiple layers of 0.1 to 0.15 mm thick ceramic layers with metal lines permitted on each layer and metal filled via holes interconnecting conductors on the different layers [2], [6]. Therefore, dense packages with RF integrated circuits, digital integrated circuits, bias lines, and interconnect lines may be built.

However, dense packages with closely spaced interconnect lines are prone to coupling or crosstalk that may severely

degrade circuit performance. Microstrip transmission lines radiate at discontinuities [7], and this radiated power may couple to other microstrip lines. In addition, parallel microstrip lines couple energy to and from each other [8]. To help alleviate this coupling, metal filled via holes are often used to create Faraday cages that isolate sections of the package from each other [9]–[12]. Three-dimensional-finite element method (3-D-FEM) electromagnetic modeling of parallel microstrip lines separated by metal filled via hole fences has shown that the fences do not reduce coupling, but if the top of the via posts are connected with a metal strip, coupling is significantly reduced [13], [20], [14].

In this paper, commercial LTCC process and design layout rules are used to experimentally verify the 3-D-FEM electromagnetic modeling results. Test circuits are built by a commercial vendor and characterized over the frequency band of 2 to 40 GHz. First, the experimental procedures are presented. Then, coupling between parallel microstrip lines are presented as a function of frequency and the via fence geometry to verify the prior 3-D-FEM results [14]. Lastly, attenuation of the microstrip lines as a function of the via fence geometry is presented. Throughout the paper, the results are quantitatively and qualitatively compared to the 3-D-FEM results.

II. CIRCUIT FABRICATION AND DESIGN

Circuits are fabricated using commercial LTCC fabrication process and layout rules [15]. The ceramic material is mounted on a Cu/Mo/Cu metal core that is thermal coefficient of expansion (TCE) matched to the LTCC dielectric, Si, and GaAs. A single layer of ceramic tape is used for the microstrip substrate. This substrate is 0.005 in (127 μm) thick, has a relative dielectric constant, ϵ_r , of 5.67 at 12.5 GHz, and a volume resistivity of $5 \times 10^{15} \Omega\text{-cm}$. According to the design rules, via holes are 0.008 in (203 μm) in diameter and have a minimum via to via spacing of 0.024 in (609 μm). All metal traces, including the microstrip lines, have a minimum conductor width and conductor-to-conductor line spacing of 0.008 in (203 μm). The metal filled vias and lines are Ag, with the lines coated with Ni/Au.

Microstrip lines are designed with a strip width, W , of 0.008 in (203 μm), which yields a theoretical characteristic impedance of 50 Ω . Referring to Fig. 1, microstrips with via to line spacing, S , of 0.012, 0.016, and 0.020 in (304, 406, and 508 μm) and via to via spacing, G , of 0.024 and 0.032 in

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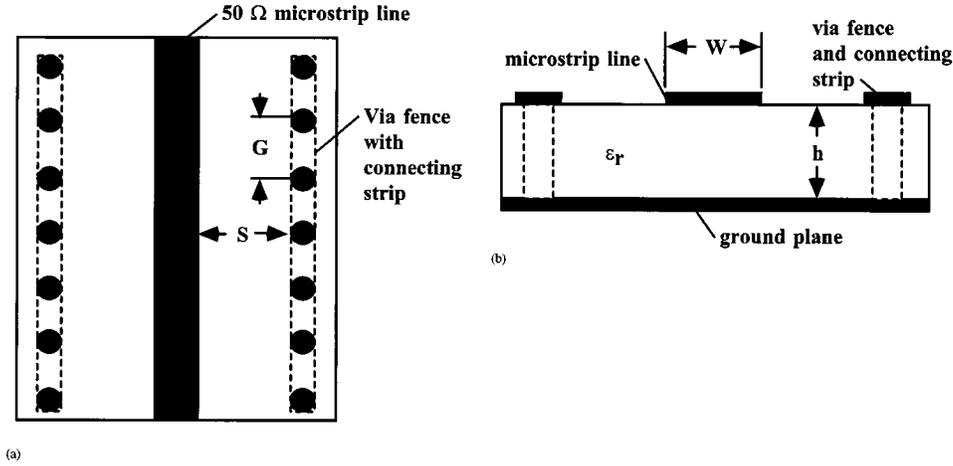


Fig. 1. (a) Top view and (b) cross section cut schematic of microstrip line surrounded by a via fence.

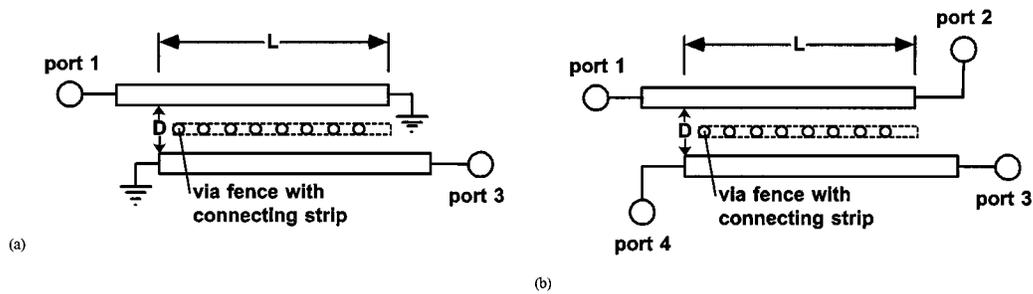


Fig. 2. Schematic of test circuits for measuring coupling between two microstrip lines is a: (a) two-port circuit and a (b) four-port circuit.

(610 and 813 μm) are fabricated both with and without a strip connecting the tops of the via holes. To maintain the same descriptions as [14], S and G are normalized to the substrate thickness, h , throughout the paper. Therefore, microstrip lines with S/h of 2.4, 3.2, and 4 and G/h of 4.8 and 6.4 are fabricated. The microstrip lines are designed with a maximum separation between the via fences, $2S + W$, that does not support quasirectangular waveguide type modes below 50 GHz. If the via fences are too far apart and higher order modes are present, the propagation characteristics are severely degraded.

Each microstrip line width is measured, and the average microstrip line width is 0.00837 in (212.7 μm). The minimum and maximum measured microstrip line width is 0.0076 in (193.0 μm) and 0.0091 in (231.1 μm), respectively. Measured strip to via spacing, S , is nominally 0.004 in (101.6 μm) less than the designed value. Microstrip metal thickness is measured to be 15 μm with a root mean square variation (surface roughness) of $\pm 4 \mu\text{m}$.

To measure the coupling between adjacent microstrip lines, two sets of circuits are characterized. The first, which is shown schematically in Fig. 2(a), consists of two short circuit terminated microstrip lines adjacent to each other. Port 1 is the input port and the coupled power is measured at Port 3. Because a standing wave is established on the short circuit terminated lines, coupling measured with this technique is 6 dB higher than the coupling as measured with a four-port circuit. Therefore, the coupling for the two-port circuits is only presented for the frequencies corresponding to peaks in the measured value of S_{13} and the values are corrected by 6 dB

so that they may be compared to the four-port results. The second set is shown schematically in Fig. 2(b) and consists of a four-port circuit that enables the measurement of the forward and backward coupling, S_{13} and S_{14} , respectively. Via fences with and without connecting strips are placed between the microstrip lines to characterize their effectiveness in reducing coupling. Microstrip line to line spacing, D/h , of 4.8 and 6.4 are characterized, and in both sets of circuits, the coupling length, L , is 0.280 in (0.7112 cm).

Measurements are made on a vector network analyzer from 2 to 40 GHz. A thru/reflect/line (TRL) calibration is implemented with MULTICAL, a TRL software program, using two delay lines of 1750 and 5000 μm and a short circuit reflect fabricated on the same substrate as the circuits. The attenuation constant of the microstrip line is determined by the TRL calibration routine [16] by comparing the measured characteristics of microstrip lines of different lengths. To improve accuracy, three sets of circuit boards were fabricated and characterized; the average of those three measurements is presented in this paper. During the measurement of the four-port circuits, two of the four ports are terminated in 50 Ω loads built into especially designed RF probes.

III. RESULTS

Fig. 3 shows the measured forward coupling between two parallel microstrip lines. The continuous lines are the measured forward coupling, S_{13} , from the four-port circuit shown in Fig. 2(b), and the discrete points are the measured forward

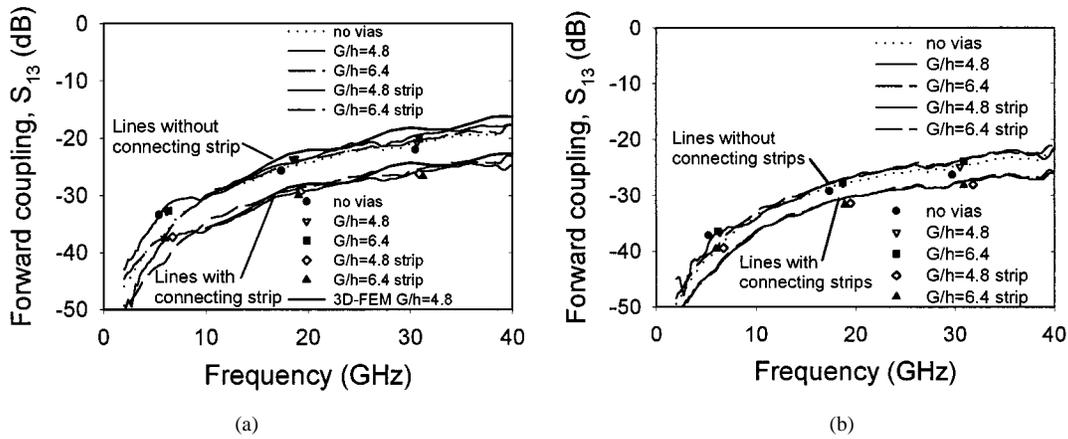


Fig. 3. Measured and 3-D-FEM calculated coupling between two microstrip lines with (a) $D/h = 4.8$ and (b) 6.4 as a function of frequency and the via fence geometry. Continuous lines are measured from the four-port circuit in Fig. 2(b) and the discrete points are measured from the two-port circuit in Fig. 2(a).

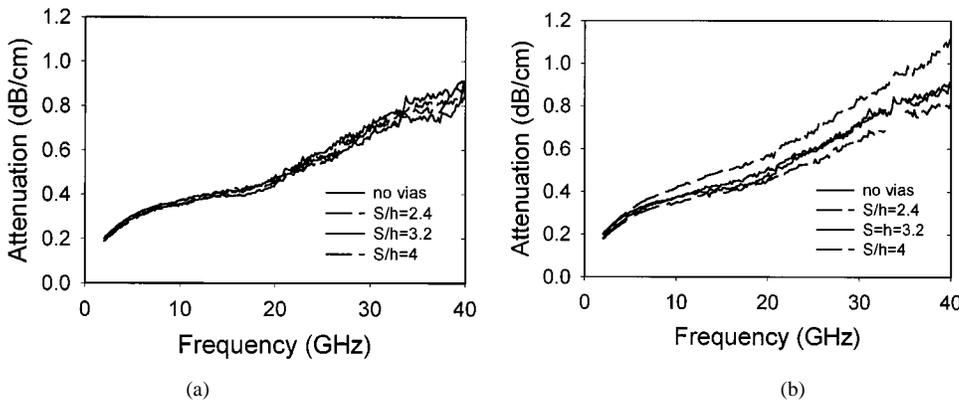


Fig. 4. Measured attenuation in dB/cm as a function of frequency of a microstrip line with no vias and microstrip lines with via fences with $G/h = 6.4$ and $S/h = 2.4, 3.2,$ and 4 (a) without a strip connecting the vias and (b) with a strip connecting the vias.

coupling from the two-port circuit shown in Fig. 2(a). The two sets of measurements are in excellent agreement, which indicates the accuracy of the measured coupling results. Also shown in Fig. 3(a) is the 3-D-FEM calculated forward coupling for a via fence with $G/h = 4.8$ without a connecting strip and with a connecting strip. There is excellent agreement between the 3-D-FEM and measured results, which quantitatively verifies the prior results from [14]. For $D/h = 4.8$ and 6.4 , it is seen that the addition of a via fence does not reduce the forward coupling, and in fact, S_{13} is one to two dB higher with the via fence compared to the microstrip without a via fence. Forward coupling is reduced by approximately 5 dB and 3 dB for $D/h = 4.8$ and 6.4 , respectively when a 0.008 in metal strip connects the tops of the via posts. All of these results are in qualitative agreement with theoretical results [14]. Notice that microstrip lines with $D/h = 4.8$ and a via fence with connecting strip have lower coupling than microstrip lines spaced 33% further apart, $D/h = 6.4$, without via fences. This decrease in coupling enables higher packing densities in RF packages. The measured maximum backward coupling, S_{14} , is 30 dB, or approximately 5 dB lower than the forward coupling. Moreover, there is no measurable dependence of S_{14} on the via hole separation.

The attenuation of the microstrip lines as a function of the via fence geometry is measured. Fig. 4(a) shows the attenuation, α ,

in dB/cm of a microstrip line with no via fence and a microstrip line with $G/h = 6.4$ and $S/h = 2.4, 3.2,$ and 4 without a connecting strip. Fig. 4(b) shows the attenuation of these same microstrip lines with a strip connecting the via fences. It is seen that the attenuation characteristics with frequency are virtually identical, with or without via fences. Attenuation is lower when microstrip is surrounded by a via fence without the connecting strip on top of the via posts because radiation loss is reduced as presented in [14]; however, when the connecting strip is added, α is higher for small S/h . Also, for all line geometry, α decreases as S/h increases. The attenuation dependence on S/h is in agreement with the theoretical results [14], but the theoretical attenuation, which only includes radiation loss, decreases when the connecting strip is added to the via fence, which is not observed in the measured results. Since significant electric fields terminate on the connecting strip when S/h is small, the propagating mode is similar to a coplanar waveguide (CPW) mode, which has higher conductor loss than similarly sized microstrip lines [17]. Therefore, the higher attenuation seen here is attributed to conductor loss. Below 20 GHz, the attenuation has a $f^{0.5}$ frequency dependence, which is expected when conductor loss dominates and the metal is smooth; however, there is an inflection point at 20 GHz where the frequency dependence becomes nearly linear. This same increase in attenuation above 20 GHz for 50 Ω microstrip lines on LTCC substrates has been

reported previously [18]. Therefore, it is not believed to be due to measurement error. Also, because the frequency characteristic of the measured attenuation is independent of the via geometry, the higher attenuation is not due to the via fences. Rather, at 20 GHz, the ratio of the surface roughness to skin depth is approximately 10, which causes significantly higher conductor loss [19].

IV. CONCLUSIONS

Using commercial LTCC packaging technology, the use of metal filled via fences to reduce the coupling between parallel microstrip lines is experimentally demonstrated. It is shown that a metal filled via fence does not reduce coupling between microstrip lines; however, if the tops of the metal filled posts are connected with a metal strip, the coupling is reduced by 5 dB. The attenuation of microstrip lines surrounded by via fences is virtually identical to the attenuation of isolated microstrip lines. These results are in agreement with the theoretical results published earlier and enable denser RF packages.

REFERENCES

- [1] R. W. Johnson, R. K. F. Teng, and J. W. Blade, Eds., *Multichip Modules Systems Advantages, Major Constructions, and Material Technologies*. New York: IEEE Press, 1991.
- [2] R. L. Brown, P. W. Polinski, and A. S. Shaikh, "Manufacturing of microwave modules using low-temperature cofired ceramics," in *Proc. 1994 IEEE MTT-S Dig.*, 1994, pp. 1727–1730.
- [3] H. Sakai, Y. Ota, K. Inoue, T. Yoshida, K. Takahashi, S. Fujita, and M. Sagawa, "A novel millimeter-wave IC on Si substrate using flip-chip bonding technology," in *Proc. 1994 IEEE MTT-S Dig.*, 1994, pp. 1763–1766.
- [4] G. White, E. Perfecto, D. McHerron, T. DeMercurio, T. Redmond, and M. Norcott, "Large format fabrication—A practical approach to low cost MCM-D," *IEEE Trans. Comp., Packag., Manufact. Technol. B*, vol. 18, pp. 37–41, Feb. 1995.
- [5] R. A. Fillion, R. J. Wojnarowski, T. B. Gorczyca, E. J. Wildi, and H. S. Cole, "Development of a plastic encapsulated multichip technology for high volume, low cost commercial electronics," *IEEE Trans. Comp., Packag., Manufact. Technol. B*, vol. 18, pp. 59–65, Feb. 1995.
- [6] R. W. Johnson, Ed., *Modular Series in Hybrid Microelectronics*. Reston, VA: Int. Soc. Hybrid Microelectronics, 1991.
- [7] N. G. Alexopoulos and S. C. Wu, "Frequency-independent equivalent circuit model for microstrip open-end and gap discontinuities," *IEEE Trans. Microwave Theory Tech.*, vol. 42, pp. 1268–1272, July 1994.
- [8] R. E. Collin, *Foundations for Microwave Engineering*. New York: McGraw-Hill, 1992, pp. 164–175.
- [9] J. W. Gippich, "EM modeling of via wall structures for high isolation stripline," in *Proc. Dig. Workshop WWFC, Interconnect Packag. Technol. Issues, IEEE Int. Microwave Symp.*, San Diego, CA, June 1994, pp. 78–114.
- [10] J. Gippich, C. Wilson, and D. Stevens, "Multilayered 3-D packaging issues," in *Proc. Dig. Workshop WFC, Interconnects Packag. RF Wireless Commun. Syst., IEEE Int. Microwave Symp.*, Denver, CO, June 8–13, 1997.
- [11] J. Gippich and D. Stevens, "Isolation characteristics of via structures in high density stripline packages," in *Proc. Dig. Workshop WME, Multilayer Microwave Circ., IEEE Int. Microwave Symp.*, Baltimore, MD, June 7–12, 1998.
- [12] M.-K. Kim, "Crosstalk control for microstrip circuits in PCB's at microwave frequencies," in *Proc. Int. Symp. Electromagn. Compat.*, 1995, pp. 459–464.
- [13] G. E. Ponchak, D. Chen, J.-G. Yook, and L. P. B. Katehi, "Filled via hole fences for crosstalk control of microstrip lines in LTCC packages," in *Proc. 3rd Int. Wireless Commun. Conf. (WCC '98) Dig.*, San Diego, CA, Nov. 1–3, 1998, pp. 96–100.

- [14] G. E. Ponchak, D. Chun, J.-G. Yook, and L. P. B. Katehi, "The use of metal filled via holes for improving isolation in LTCC RF and wireless multichip packages," *IEEE Trans. Adv. Packag.*, vol. 23, pp. 88–99, Feb. 2000.
- [15] *DiPak Design Guidelines*, Dielectric Laboratories, Inc., 2000.
- [16] D. F. Williams, R. B. Marks, and A. Davidson, "Comparison of on-wafer calibrations," in *Proc. 38th ARFTG Conf. Dig.*, San Diego, CA, Dec. 5–6, 1991.
- [17] I. Bahl and P. Bhartia, *Microwave Solid State Circuit Design*. New York: Wiley, 1988.
- [18] *DiPak Millimeter Wave Package DC-40 GHz Product Description*, Dielectric Laboratories, Inc., 2000.
- [19] C. L. Holloway and E. F. Kuester, "Power loss associated with conducting and superconducting rough interfaces," *IEEE Trans. Microwave Theory Tech.*, vol. 48, pp. 1601–1610, Oct. 2000.
- [20] G. E. Ponchak, D. Chen, J.-G. Yook, and L. P. B. Katehi, "Filled via hole fences for crosstalk control of microstrip lines in LTCC packages," in *Proc. IMAPS 1998 31st Int. Symp. Microelectron.*, San Diego, CA, Nov. 2–4, 1998.



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