

# Monolithic Wilkinson Power Divider on CMOS Grade Silicon With a Polyimide Interface Layer for Antenna Distribution Networks

George E. Ponchak, *Senior Member, IEEE*, Andrew Bacon, and John Papapolymerou, *Member, IEEE*

**Abstract**—Using an optimized finite ground coplanar waveguide layout on a CMOS grade silicon wafer with a 20- $\mu\text{m}$ -thick polyimide interface layer and embedded passives, a Wilkinson power divider is built. The measured characteristics show an insertion loss of only 0.57 dB at 12.5 GHz and better than 15 dB return loss and isolation.

**Index Terms**— Coplanar waveguide (CPW), planar transmission lines, power divider, silicon, Wilkinson.

## I. INTRODUCTION

WITH the development of SiGe heterojunction bipolar transistors with a high frequency of oscillation, a strong interest has developed in RF and microwave monolithic integrated circuits (RFIC and MMIC) integrated with digital circuits on the same chip. Ideally, to lower cost and enable the circuits to be fabricated in high volume, standard CMOS integrated circuit processing is desired. However, traditional distributed microwave circuit designs reliant on transmission lines have high loss due to the low resistivity of the silicon substrate commonly used for BiCMOS and CMOS integrated circuits [1].

To overcome this problem, dielectric layers, such as polyimide, can be used on top of the CMOS substrate to create an interface layer that can host low-loss microwave components. Both microstrip and coplanar waveguide transmission lines fabricated this way have exhibited low attenuation for an optimum polyimide thickness [1]–[3]. Recently, finite ground coplanar (FGC) waveguide folded-slot antenna [4] and filters [5] have been demonstrated on such a substrate configuration.

Wilkinson power dividers are often used in antenna distribution networks and power amplifiers when in-phase power division/combining is required. A lumped element, 1.8-GHz Wilkinson power divider on CMOS grade Si using a 25- $\mu\text{m}$ -thick  $\text{SiO}_2$  interface layer [6] and a distributed, 15-GHz, hybrid Wilkinson power divider with a wire-bonded chip resistor on CMOS grade Si and a 20- $\mu\text{m}$  polyimide interface layer have been reported [7].

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G. Ponchak is with the NASA Glenn Research Center, Cleveland, OH, 44135 USA.

A. Bacon and J. Papapolymerou are with the School of Electrical and Computer Engineering, Georgia Institute of Technology, Atlanta, GA 30332-0250 USA (e-mail: papapol@ece.gatech.edu).

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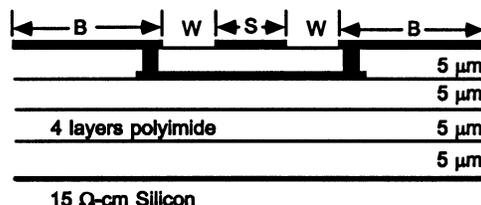


Fig. 1. Cross-sectional schematic of the finite ground coplanar waveguide (CPW) lines on CMOS Si with a polyimide interface layer.

In this paper, we report for the first time a monolithic design and implementation of a distributed Wilkinson power divider on CMOS grade Si with a polyimide interface layer and embedded passives that yield significantly lower insertion loss. Measured characteristics are presented and compared to the ideal and 2.5-D method of moments (MoM) circuit characteristics derived with Sonnet software.

## II. CIRCUIT DESIGN

The FGC line geometry is chosen to yield the lowest loss on a 15- $\Omega$  – cm Si wafer with 20  $\mu\text{m}$  of polyimide [2]. Referring to Fig. 1,  $S$ ,  $W$ , and  $B$  are 74, 8, and 222  $\mu\text{m}$ , respectively, for the 50  $\Omega$  lines and 42, 16, and 126  $\mu\text{m}$  for the 70.7  $\Omega$  lines. This optimization was not possible in [7], as the lines had to conform to the bonding wire tolerances. A MoM analysis implemented through *Sonnet* software is used to determine the characteristic impedance and effective permittivity  $\epsilon_{\text{eff}}$  of the FGC lines. Using the MoM predicted  $\epsilon_{\text{eff}}$ , the hybrid junction is designed around the center frequency of 15 GHz using ideal transmission line analysis with no correction for FGC line dispersion or parasitic reactance caused by the “T” junctions, the 90° bend, and the bridges. Fig. 2 shows the Wilkinson power divider layout.

A 20- $\mu\text{m}$ -thick layer of Dupont PI-2611 polyimide is spun onto the wafer in four, 5- $\mu\text{m}$ -thick layers. Each layer is fully cured at 340 °C for 120 min before the next layer is added. PI-2611 polyimide has a relative dielectric constant of 3.12 measured at 1 MHz [8] and a loss tangent of 0.002 measured at 1 kHz [9]. The circuit is fabricated on the top surface and the bridges required to tie the ground planes together at the “T” junctions, the 90° bend, and at the resistor, as shown in Fig. 2, are fabricated on the third layer, which is 15  $\mu\text{m}$  from the Si as shown in Fig. 1. Via holes through the fourth, 5- $\mu\text{m}$ -thick layer connect the two layers. A thin film, Ti resistor is evaporated on the top surface of polyimide. The complete circuit is monolithic.

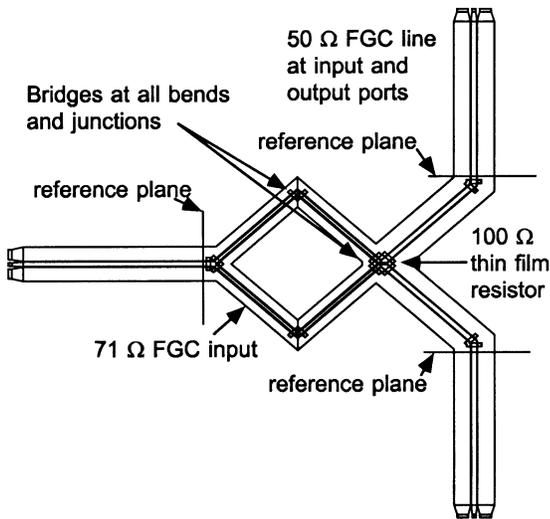


Fig. 2. Circuit layout of Wilkinson power divider.

### III. MEASUREMENT TECHNIQUE

The FGC propagation characteristics are measured with an 8510C vector network analyzer and probe station. A quartz spacer between the Si substrate and the probe station wafer chuck is used to eliminate parasitic microstrip and parallel-plate waveguide modes during testing. The propagation constant  $\gamma = \alpha + j\omega\sqrt{\epsilon_{eff}}/c$ , where  $\alpha$  is the attenuation constant,  $\omega$  is the angular frequency, and  $c$  is the velocity of light in vacuum, is de-embedded through the thru-reflect-line (TRL) calibration routine implemented in the software program MULTICAL [10]. For each FGC line characterized, four delay lines with the longest line being 1 cm are used in addition to the thru line to enhance accuracy from 1 to 30 GHz. The reference planes are shown in Fig. 2. During characterization, one of the ports is terminated with RF probes with integrated 50- $\Omega$  terminations.

### IV. RESULTS

The measured propagation characteristics of the 50 and 70.7  $\Omega$  lines were measured first to verify the design. For the 70.7  $\Omega$  line, which determines the circuit frequency, the MoM, and the measured  $\epsilon_{eff}$  at 15 GHz are 2.50 and 2.46, respectively, which is in very good agreement. At 15 GHz, the measured attenuation of the 50 and 70.7  $\Omega$  FGC lines is 2.67 and 1.89 dB/cm, respectively. Since the reference planes at the output ports are 0.16 cm from the junction, as shown in Fig. 2, 0.43 dB of extra insertion loss is included in the characteristics of the Wilkinson circuit. Based on the measured attenuation of the 70.7  $\Omega$  lines, the  $\lambda/4$  line sections of the hybrid junction each contribute 0.59 dB of insertion loss.

The measured, modeled, and *Sonnet* results for the power divider are shown in Figs. 3–7. First, it is seen that the measured characteristics match the ideal circuit characteristics very well except for the FGC line insertion loss and a slight shift in the center frequency. Since the measured and modeled  $\epsilon_{eff}$  agreed well, the frequency shift is due to the parasitic reactance at the “T” junction, the 90° bends, and the area around the resistor. The *Sonnet* MoM simulations of the circuit shown in Figs. 1 and 2 agree very well with the measured data, indicating that the loss

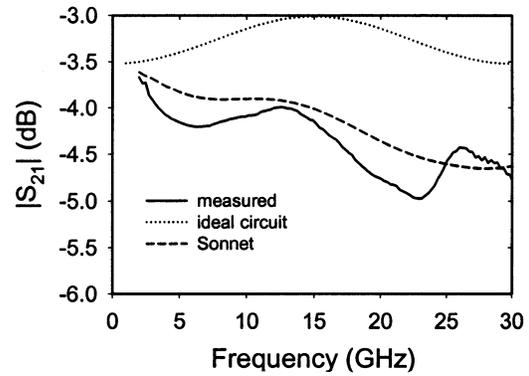


Fig. 3. Measured and modeled through characteristics  $|S_{21}|$ .

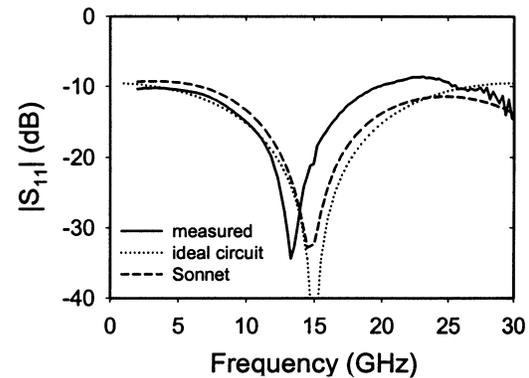


Fig. 4. Measured and modeled input port return loss.

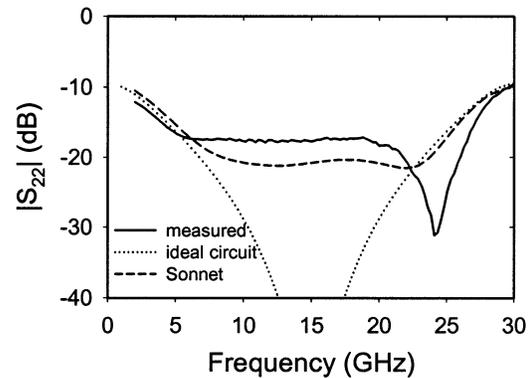


Fig. 5. Measured and modeled output port return loss.

is accounted for by the metal and Si resistivity. The measured insertion loss is 1 dB, which is a 5 dB improvement over the prior art [7] when comparing at the measured resonant frequencies of the two dividers. When the comparison is made at 12.5 GHz, the loss is improved by 2 dB. If the insertion loss of the feed lines at the output ports is subtracted, the power divider has 0.57 dB of loss. Furthermore, since 1.02 dB of loss is accounted for in the FGC lines, no power is lost to surface waves, radiation, or coupling to slotline modes. The return loss is 15 dB or higher at all three ports as shown in Figs. 4 and 5 and the isolation between ports 2 and 3 is 20 dB as shown in Fig. 6. Loss results are summarized in Table I. Finally, the phase characteristics are shown in Fig. 7, where it is seen that the phase response is nearly linear across the measured frequency band.

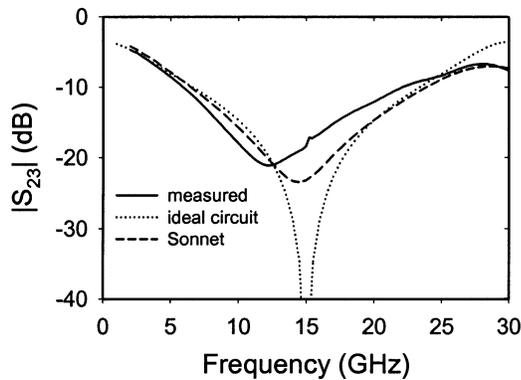


Fig. 6. Measured and modeled isolation between output ports.

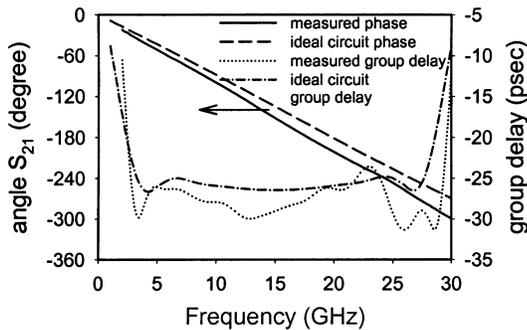


Fig. 7. Measured and modeled  $S_{21}$  phase characteristics.

TABLE I  
LOSS RESULTS FOR THE WILKINSON DIVIDER AT 12.5 GHz

Parameter	Value (dB)
Measured $S_{21}$	4
Ideal $S_{21}$	3
Divider loss at reference planes	1
Line loss between T-junction and reference planes	0.43
Divider loss at T-junction	0.57
Return loss	26

Overall, the monolithic divider presented here has a superior performance to that of [7], because no bonding wires are used to connect the resistor and the FGC line dimensions are optimized for low loss instead of accommodating the bond wire and chip resistor tolerances and geometry. The small differences in the

FGC line impedances between the monolithic and hybrid approaches cannot account for the 5 dB improvement in insertion loss.

V. CONCLUSION

A Wilkinson power divider on a CMOS grade Si wafer has been demonstrated with only 0.57 dB of insertion loss at 12.5 GHz, which is a 2 dB reduction over the prior art (5 dB when comparing at the resonant frequencies). This improvement is due to the use of embedded resistors and air bridges and the optimization of the transmission lines.

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