

Low Loss, Finite Width Ground Plane, Thin Film Microstrip Lines on Si Wafers

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ABSTRACT

Si RFICs on standard, 2 Ω -cm Si wafers require novel transmission lines to reduce the loss caused by the resistive substrate. One such transmission line is commonly called Thin Film Microstrip (TFMS), which is created by depositing a metallic ground plane, thin insulating layers, and the microstrip lines on the Si wafer. Thus, the electric fields are isolated from the Si wafer. In this paper, it is shown through experimental results that the ground plane of TFMS may be finite width and comparable to the strip width in size while still achieving low loss on 2 Ω -cm Si. Measured effective permittivity shows that the field interaction with the Si wafer is small.

INTRODUCTION

Si Radio Frequency Integrated Circuits (RFICs) are progressing rapidly into the wireless communication and automobile sensor markets, due in large part to significant improvements in SiGe HBTs. However, RF transmission lines on Si substrates suffer from high loss unless novel transmission lines or high resistivity Si wafers are used [1]. On low resistivity, 0.1 to 10 Ω -cm, Si wafers such as commonly used for CMOS and Bi-CMOS circuits, Thin Film Microstrip (TFMS) has been shown to have low loss [2], and it may be manufactured using standard Si processing steps to create Si RFICs [3].

A schematic of TFMS is shown in Figure 1. Typically, a large area of the topside of the Si wafer is metallized and this serves as the ground plane for the TFMS. Thus, the ground plane width, G , is very large and may be considered infinite. This assures that there will be no electric field interaction with the Si wafer and the high loss associated with it. On top of the ground plane, a thin layer of insulating material is

deposited to serve as the microstrip substrate. Since polyimide may be deposited in multiple layers of 1 to 20 μ m thick and it is used for planarization during Si IC processing, it is often used for the substrate of TFMS lines. Finally, the microstrip circuit is defined on top of the polyimide.

In this paper, we introduce a finite width ground plane TFMS line. Measured attenuation of TFMS show that the ground plane only needs to be 3 to 5 times the strip width, W . Furthermore, measured effective permittivity shows that the finite width ground planes shield the electric fields from the Si wafer. A 2D- Finite Element Method (FEM) analysis is included to compute the electric fields and propagation constant of the new lines. It is believed that these narrow, TFMS lines will enable the production of smaller Si RFICs, which will give them a larger cost advantage compared to GaAs and InP circuits.

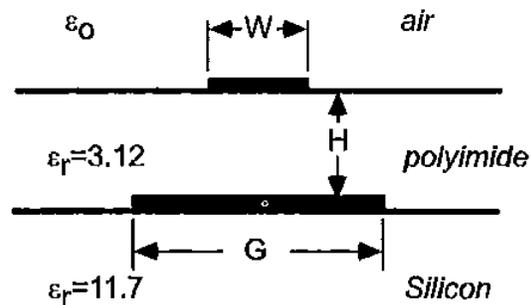


Figure 1: Schematic of Thin Film Microstrip (TFMS).

EXPERIMENT

To characterize the propagation characteristics of TFMS on Si substrates, test structures are fabricated on a single wafer. A ground plane consisting of a 200 \AA Ti adhesion

layer, 1.5 μm of Au, and a 200 \AA Cr cap layer is defined on an n-type, 0.5 to 2.5 $\Omega\text{-cm}$ Si wafer. This is followed by spinning on DuPont adhesion promoter and PI-2611 polyimide and curing it at 350 C for 60 minutes. PI-2611 has a relative dielectric constant, ϵ_r , of 3.12 [4] measured at 1 MHz and a loss tangent of 0.002 [5] measured at 1 kHz. The finite width ground planes create a nonplanar surface, which is partially planarized by the polyimide, resulting in the polyimide being 11.25 μm thick where there is no ground plane and 11.05 μm thick over the ground planes ($H=11.05 \mu\text{m}$). Ni is used as a hard mask to Reactive Ion Etch (RIE) via holes in the polyimide for topside connection to the ground planes. Finally, a lift off process is used to fill the via holes, define the probe pads, and the microstrip lines in a single step; 200 \AA Cr and 1.6 μm of Au is used. These dimensions are confirmed through 3D-profiler and SEM measurements, which also show that surface roughness is small enough to be neglected.

The microwave characterization is performed over the frequency range of 2 to 40 GHz using a HP 8510C vector network analyzer and GGB Industries RF probes. To extract the attenuation and effective permittivity, ϵ_{eff} , of the TFMS, a Thru-Reflect-Line (TRL) calibration routine implemented through the NIST MULTICAL software routine is used. TRL calibration routines use extra data measured during calibration to determine the propagation characteristics of the delay lines. Each set of calibration standards consists of a 5000 μm thru line, a short circuit reflect, and delay lines of 6800, 7400, 9800, and 15000 μm length. The advantage of the MULTICAL TRL calibration routine is that it uses the weighted average of all four-delay lines at each frequency point to increase accuracy. To improve probe placement accuracy, the probe pads are designed to assure probe placement within 15 μm , which results in a worst case error of 0.6 percent due to probe placement errors.

THEORETICAL ANALYSIS

The theoretical analysis of the TFMS lines was performed using an FEM solver [7]. The problem set up is shown in Figure 1, where a 2 $\Omega\text{-cm}$ Si wafer with thickness of 500 μm has been

used as a substrate. The whole structure is surrounded by a radiation boundary that simulates the region outside the drawing space as being infinitely large, thus isolating the model from other voltage or charge sources. An initial coarse mesh consisting of triangular elements is created at the beginning of the solution process. The discretization of the problem area is adaptively refined until the solution converges; i.e. the energy changes between two consecutive passes are small.

From the computed values of the electric field at the nodes of the triangular elements, two-dimensional contour plots of the magnitude of the electric field are generated. Additional parameters like the effective permittivity and the characteristic impedance are extracted. Initially, the capacitance of the TFMS line is computed by integrating the dot product of the electric field and the electric flux density over the cross-section of the structure. By solving the problem once without the dielectric and once with the dielectric, the characteristic impedance, Z_c , and the effective permittivity, ϵ_{eff} , are evaluated from the following equations:

$$Z_c = \frac{1}{c\sqrt{C_{\text{diel}}C_0}}, \quad \epsilon_{\text{eff}} = \frac{C_{\text{diel}}}{C_0}$$

where $c=3 \cdot 10^8$ m/sec.

MEASURED TFMS CHARACTERISTICS

TFMS lines are characterized for line widths of 23 and 52 μm . Employing standard microstrip design equations for infinite width ground planes and the polyimide thickness of 11.05 μm , these TFMS lines have a characteristic impedance of 53 and 31 Ω respectively. Using Maxwell 2D simulator, the characteristic impedance is calculated to be 52.47 and 30.28 Ω respectively at 20 GHz. Ground plane widths, G , of 2W, 3W, 5W, and 9W are characterized. The measured attenuation of these lines is shown in Figure 2. Although TFMS is considered a lossy transmission line, a minimum attenuation of approximately 3 dB/cm is achieved, which is lower than similarly sized CPW lines on GaAs or Si with a resistivity greater than 2500 $\Omega\text{-cm}$ [1]. Across the measured frequency spectrum, the attenuation decreases as the ground plane width

increases; however, the difference between very wide ground planes ($G=9W$) and narrow ground planes ($G=2W$) is less than 0.8 dB/cm for the 53 Ω line and 0.5 dB/cm for the 31 Ω line at 40 GHz. Figure 3 shows the measured attenuation at 20 GHz as a function of G/W and W . It is seen that a ground plane width greater than $3W$ is required for low attenuation for both the 31 and 53 Ω lines, and wider ground planes do not lower attenuation significantly.

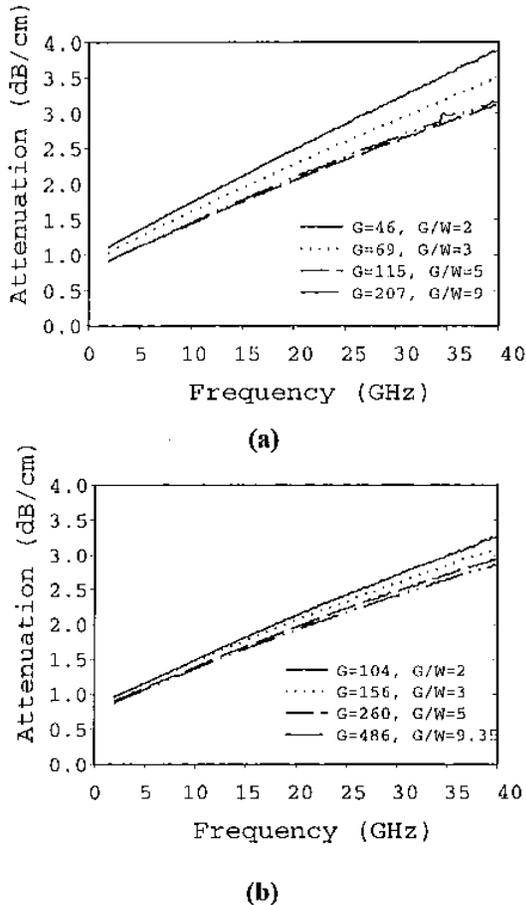


Figure 2: Measured attenuation of TFMS lines as a function of frequency with (a) $W=23 \mu\text{m}$ and (b) $W=52 \mu\text{m}$.

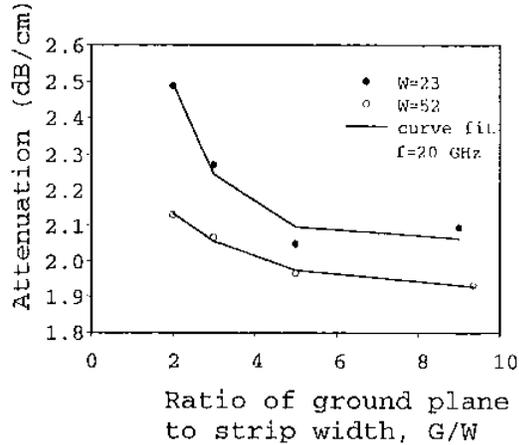


Figure 3: Measured attenuation at 20 GHz of TFMS as a function of the ground plane width to strip width.

The associated effective permittivity is shown in Figure 4 where it is seen that ϵ_{eff} is greater for narrow ground plane lines; however, ϵ_{eff} does not change for ground plane widths greater than $3W$. Theoretical analysis predicts an effective permittivity of 2.605 and 2.825 at 20 GHz for the TFMS with $W=23$ and $52 \mu\text{m}$ respectively and $G/W=5$. It is noted that the theoretical and measured ϵ_{eff} agree to within 4 percent; however, this agreement can be improved by modifying the polyimide relative dielectric constant within the published range of values and carefully including metal resistivity and internal inductance in the analysis.

The measured results show that narrow ground plane microstrip lines on CMOS grade Si may be used without a penalty in attenuation, but the origin of the attenuation has not been determined. Because there is excellent agreement between the theoretical and measured results, it is possible to use the theoretical analysis to answer that question. There are two possibilities for the higher loss when $G/W < 3$: high electric field concentrations in the Si where they would be attenuated due to dielectric losses, and higher conductor loss in the ground planes because of higher current density. Note that the measured effective permittivity shown in Figure 4 indicates electric fields in the Si for narrow ground planes, but the slope of ϵ_{eff} as a function of frequency indicates conductor loss also plays a role.

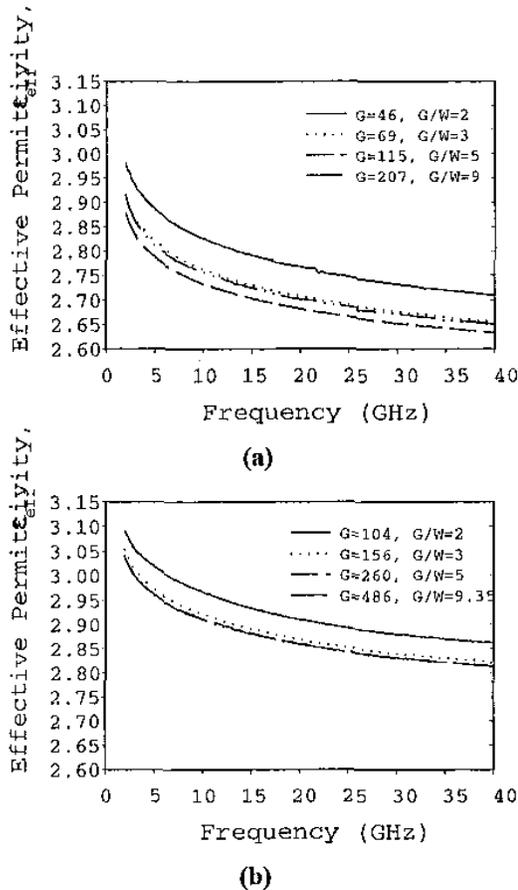


Figure 4: Measured effective permittivity of TFMS lines as a function of frequency with (a) $W=23 \mu\text{m}$ and (b) $W=52 \mu\text{m}$.

Using the 2D electromagnetic simulator, the electric fields for the transmission line may be determined. This is shown for two microstrip lines in Figure 5. The electric field magnitude of a microstrip line with $G/W=2$ and $G/W=3$ are shown in Figures 5a and 5b respectively. It is clearly seen that most of the electric fields are concentrated immediately below the microstrip line. In Figure 6, the maximum electric field magnitude in the Si substrate at 20 GHz is shown as a function of G/W . It is seen that $|E|_{\text{max}}$ decreases as G/W increases, regardless of the strip width. It is also noted that $|E|_{\text{max}}$ as a function of G/W has the same relationship as attenuation as a function of G/W as shown in Figure 3.

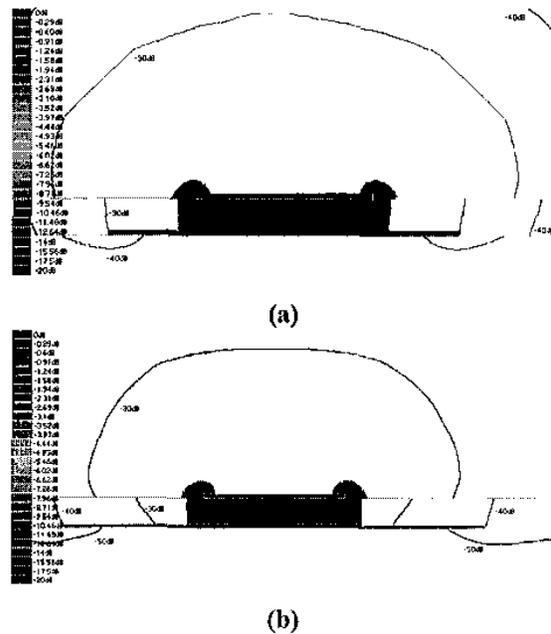


Figure 5: Calculated electric field magnitude of finite width ground plane microstrip, $W=52 \mu\text{m}$ and (a) $G/W=2$, (b) $G/W=3$.

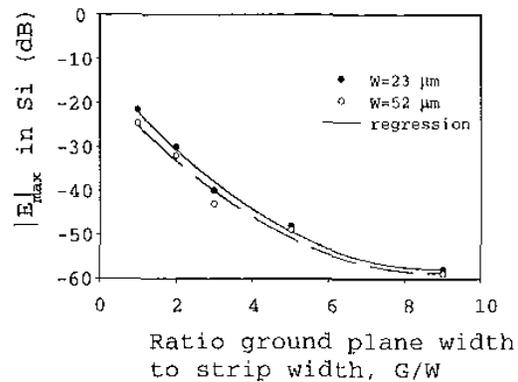


Figure 6: Calculated maximum electric field in the Si substrate at 20 GHz as a function of the strip width and G/W .

The electromagnetic simulator may also be used to determine the current density on the ground plane. In Figure 7, the current density at 20 GHz on the ground plane of microstrip lines with $W=20 \mu\text{m}$ is shown as a function of the ground plane width. It is seen that the current density decays rapidly as the ground plane width increases, and that it increases again at the edge of the ground strip.

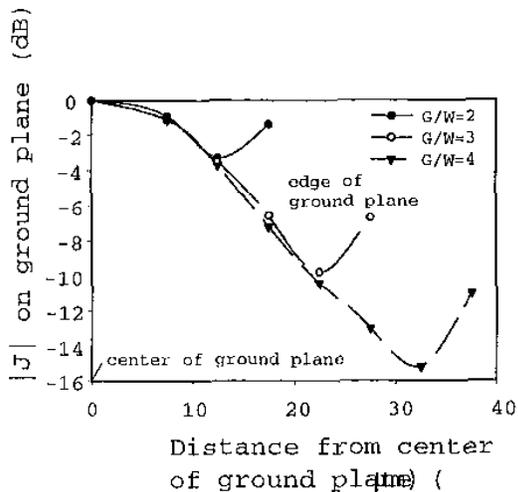


Figure 7: Current density on the ground plane as a function of G/W .

Based on the results presented in Figures 6 and 7, the attenuation is dominated by conductor loss in the narrow ground planes and not dielectric loss in the Si. Note that the electric fields in the Si are 30 dB below the maximum electric field directly under the microstrip line even for narrow ground plane widths, and it is not reasonable to assume measurable differences in loss for that low of a value. On the other hand, the current density on the ground plane indicates that there is higher conductor loss for narrow ground planes due to high current density on the metal edges.

CONCLUSIONS

Through measured propagation characteristics of TFMS lines on 2.5 Ω -cm Si wafers, it is shown that the ground plane may be reduced to 3W without any increase in attenuation. Theoretical analysis shows that even this narrow of a ground plane shields the electric fields from the Si wafer. Furthermore, higher loss for narrower ground strips is due to conductor loss. Thus, the area required for the transmission lines is reduced compared to standard TFMS with infinite, or very wide ground planes, and more of the Si wafer is available for active components such as SiGe HBTs and lumped passive elements. Therefore, it should be possible to reduce the size of Si RFICs.

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REFERENCES

1. G. E. Ponchak, "RF transmission lines on silicon substrates," *29th European Microwave Conference Dig.*, Munich, Germany, Oct. 5-7, 1999, pp. 158-161.
2. G. E. Ponchak and A. N. Downey, "Characterization of thin film microstrip lines on polyimide," *IEEE Trans. Components, Packaging, and Manufacturing Tech. -Part B*, Vol. 21, No. 2, pp. 171-176, May 1998.
3. I. Toyoda, K. Nishikawa, T. Tokumitsu, K. Kamogawa, C. Yamaguchi, M. Hirano, and M. Aikawa, "Three-dimensional masterslice MMIC on Si substrate," *IEEE Trans. Microwave Theory and Tech.*, Vol. 45, No. 12, pp. 2524-2530, Dec. 1997.
4. J. Leu, H.-M. Ho, J. K. Lee, J. Kasthurirangan, C. N. Liao, and P. S. Ho, "The evaluation of low dielectric constant materials for deep submicron interconnect applications," in *Proc. 6th Meeting DuPont Symposium Polyimides Microelectronics*, May 1-3, 1995.
5. DuPont Company Pyralin LX data sheet.
6. R. B. Marks, "A multilane method of network analyzer calibration," *IEEE Trans. Microwave Theory and Tech.*, Vol. 39, No. 7, pp. 1205-1215, July 1991.
7. Maxwell 2D simulator, Ansoft Corporation, Pittsburgh, PA.