An 8.4 GHz SiGe/Si HBT-Based MMIC Power Amplifier

Zhenqiang Ma[†], Saeed Mohammadi [†], Pallab Bhattacharya[†], Linda P. B. Katehi[††],
Samuel A. Alterovitz[†††], and George E. Ponchak[†††]

[†]Department of Electrical Engineering and Computer Science, University of Michigan, Ann Arbor, MI 48109-2122
[††]College of Engineering, Purdue University, West Lafayette, IN 47907-1280
[†††]NASA Glenn Research Center, 21000 Brookpark Road, Cleveland, OH 44135

ABSTRACT: A single-stage X-band MMIC power amplifier incorporating a SiGe/Si power HBT and lumped passive components is reported. The power HBT is characterized by an f_{max} of 67 GHz and a BV_{CBO} of more than 24 V. The matching circuits were designed for maximum output power using on-chip spiral inductors and SiO MIM capacitors. Continuous wave measurements were made at 8.4 GHz, under class A operation. The power amplifier demonstrated a linear gain of 8.6 dB, output power at peak efficiency of 22.9 dBm and a saturated output power of 24.8 dBm.

I. INTRODUCTION

The development of high-speed Si/SiGe HBTs has been accelerated in recent years. With both f_T and f_{max} being shot to 200 GHz, SiGe/Si HBTs have proven to be suitable for most microwave applications. Driven by cost and ease of integration with CMOS, Si-based monolithic microwave integrated circuits (MMIC) have received considerable attention. A number of MMICs with SiGe/Si HBTs as the active components have been reported, such as voltage-controlled oscillators (VCO's) [1], X-band mixers [2], narrow-band amplifiers at X-, Ku- [3] and Ka-band [4] and wide-band amplifiers [5]. However, high-frequency MMIC power amplifiers using SiGe/Si HBTs have not been reported. The successful development of high-performance MMIC power amplifiers relies on the availability of high-performance power SiGe/Si HBTs and high-Q factor on-chip passive components. In this paper, we report the demonstration of an X-band (8.4 GHz) MMIC high power amplifier using SiGe/Si HBT and lumped passive components.

II. DEVELOPMENT OF SiGe/Si POWER HBTS

The important requirements and considerations for the design of suitable HBTs for the present application have been described in Ref. 6. The design goal for a power HBT is to achieve high-frequency operation while maintaining high power handling capability. The design of the collector region has the most significant effects on the overall performance of a power HBT [7]. It has been realized [6] that a high breakdown voltage with low current density, which can be obtained by designing a thick and lightly-doped collector layer (limited by the Kirk effect), is preferred for power HBT design. Although a thicker collector layer will result in a larger delay time τ_{EC}, and thus lower f_T, a high f_{max}, which is a better performance indicator than f_T in evaluating microwave power devices, can still be achieved by optimizing the device design. The dependence of f_{max} on collector layer thickness has been identified and formulated by us in Ref. 6 and the previous experimental proof of this dependence can be found in Ref. 8.

The HBT heterostructure was grown on high-resistivity (10^4 ohm-cm) 4 in. Si wafers by chemical vapor deposition (CVD). The measured SIMS profile of the heterostructure is shown in Fig. 1, with a maximum boron doping concentration of 2.4×10^{19} cm^{-3} in the base region.

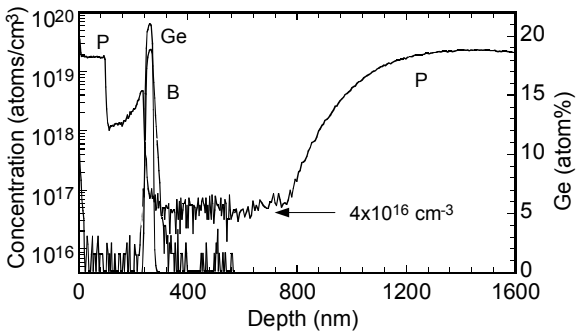

Fig. 1. Measured SIMS profile in a CVD-grown device.

A proper device layout design can minimize thermal effects in power HBTs. A detailed discussion of the parameter selection rules for multi-finger configuration can be found in Ref. 9. A self-aligned base-emitter structure is used to reduce the base access resistance. The finger spacing is a critical parameter since a balance between thermal effects and high frequency performance ($C_{BC}\rightarrow f_{max}$) is directly related to this parameter. A compromise can be made by dividing all the emitter fingers into several subcells, in each of which several fingers with narrow finger spacing are bound together. This configuration can reduce thermal effects without increasing C_{BC}, but with the extra advantage of decreased collector spreading resistance. The emitter parameters need to be carefully chosen and in our case the finger width is 2 μm, finger length is 30 μm, the finger spacing is 2 μm and there are 2 fingers in each subcell. The subcell spacing was designed to be 10 μm, leading to a temperature increase within the acceptable range. Collector metal is formed between subcells with an interdigitated configuration. The actual emitter area of a 10-finger HBT is 600 μm^2. The fabrication process of double-mesa type discrete HBTs has been described by Rieh *et al* in Ref. 3. Figure 2 shows the micrograph of a finished 10-finger common-base HBT.

High breakdown voltages were measured from the devices with 24 V BV_{CBO} and about 20 V BV_{CEO}. 10-finger common-emitter devices show an f_T of over 20 GHz. Devices in the common-base (CB) configuration show better high-frequency performance than common-emitter (CE) devices with an identical active area layout, mainly because the frequency-limiting capacitance C_{EC} in CB configuration is smaller than C_{BC}

in CE configuration. The high-frequency response characteristics of a 10-finger common-base HBT are shown in Fig. 3. A measured f_{max} of 39 GHz (it can be extrapolated to 67 GHz based on 6dB/octave roll-off) was achieved. The maximum stable gain (G_{max}) is 16.7 dB at 8.4 GHz.

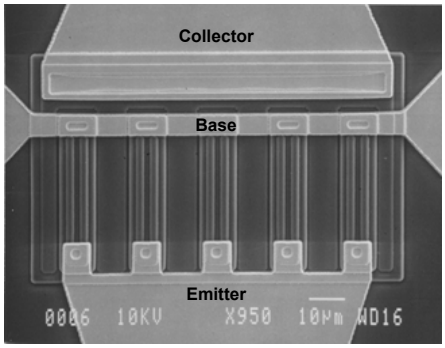

Fig. 2. Photomicrograph of a 10-finger common-base SiGe/Si HBT with emitter area of 780 μm^2 and interdigitated collector electrode metals.

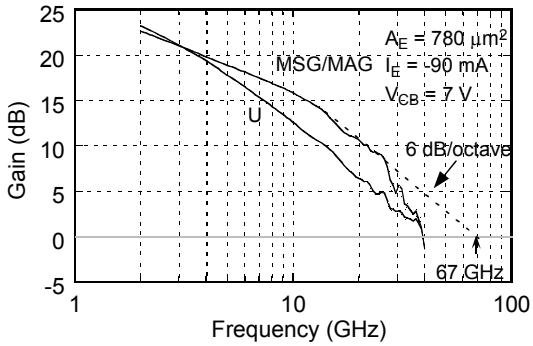

Fig. 3. Small-signal characteristics of a 10-finger CB SiGe/Si HBT.

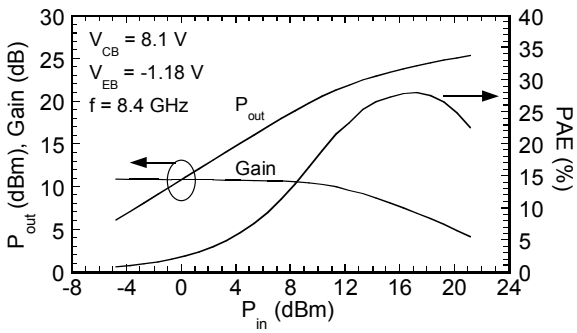

Fig. 4. Power performance of 10-finger CB SiGe/Si power HBT. ($\Gamma_S = 0.64\angle 178^o$ and $\Gamma_L = 0.71\angle 85^o$)

The large-signal performance of the 10-finger CB SiGe HBT was tested on wafer at 8.4 GHz using a single-tone Focus Microwave load-pull system under class AB operation in CW mode. No special arrangement for heat dissipation was employed in the measurements. The device was biased for class AB operation and the matching was optimized for maximum output power. The measured output power P_{out}, gain and power added efficiency PAE are plotted as a function of input power P_{in} in Fig. 4. The measured linear gain is 10.9 dB. At 1 dB and 3 dB gain compression, the RF output power P_{1dB} and P_{3dB} are 21.5 dBm (140 mW) and 23.5 dBm (224 mW), respectively. The maximum PAE, 28%, is achieved at 4 dB gain compression with associated RF output power of 24.2 dBm (263 mW). The saturated RF output power is as high as 26.3 dBm (430 mW, 0.55 mW/μm^2 power density). Higher PAE could be obtained if the measurement is optimized for this purpose.

III. POWER AMPLIFIER DEVELOPMENT

An accurate large-signal model is required for the design of a power amplifier circuit. The conventional Gummel-Poon model was used to model the power HBT in this study. Since the thermal effects have been minimized from the optimal device design (also due to the large-thermal conductivity of Si), a thermal circuit-free model with fair accuracy has been generated. The detailed model procedure and results can be found in our previous publication [6].

The lumped passive components, including spiral inductors, MIM capacitors and thin film resistors, are important on-chip circuit components for MMIC applications. These components possess the advantage of smaller size than the distributed transmission lines at X-band frequencies. The low Q-factor of on-chip (particularly on Si) spiral inductors can significantly limit the circuit performance, which has been a major obstacle to realize Si-based MMIC power amplifiers at X-band. In order to improve the Q-factor of spiral inductors, micromachined structures have been developed. By removing the substrate material underneath the inductor metal line using controlled isotropic dry etching, the Q-factor and resonance frequency of spiral inductors have been greatly improved [3].

Circuit simulation and optimization were performed with HP EESOF LIBRA. The detailed fabrication process of the MMIC circuits has been described by Rieh *et al* [3]. The on-chip matching networks were realized with the micromachined spiral inductors and SiO MIM capacitors. The input and output matching networks were designed for high output power. The photomicrograph of the fabricated MMIC power amplifier is shown in Fig. 5. The small chip size of 1 x 0.6 mm^2 results from the use of lumped passive elements.

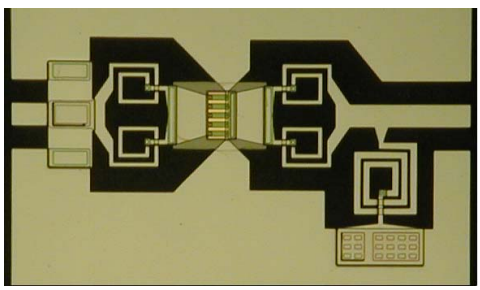

Fig. 5. Photomicrograph of a fabricated MMIC power amplifier.

The fabricated power amplifier was tested on-wafer under continuous wave (CW) operation (class A) at room temperature. Figure 6 shows the measured bias-dependent small-signal gain

and input/output return losses of the power amplifier. At 8.4 GHz and with a bias of I_E = -95 mA and V_{CB} = 7 V, the small-signal gain is 8.6 dB, with input and output return loss of 6 dB and 11.6 dB, respectively. The peak gain is smaller than the designed value (~10 dB). A detailed investigation after the circuit characterization shows that the Q-factors of the passive components, which were incorporated in the circuit, are lower than the desired values. The low-Q factors were further identified to be due to high serial parasitic resistance and it can be easily improved with better processing techniques. Figure 7 shows the output power, gain and power added efficiency (PAE) as a function of input power, measured at 8.4 GHz, with the HBT biased at V_{EB} = -1.3 V and V_{CB} = 11.5 V (class A) for maximum output power. This high operation voltage is a consequence of the high-breakdown voltage achieved with a thick and lightly doped collector layer. The peak efficiency, 12% at these bias conditions was achieved at 2.9 dB gain compression. The output power at the peak value of PAE is 22.9 dBm (195 mW) and 24.8 dBm (302 mW) in its saturation. These values, particularly the PAE, are also lower than the designed values for the same reasons as mentioned above for the small-signal characteristics. The major loss comes from resistive loss associated with the spiral inductors. Although the design of the circuit was optimized for maximum output power, higher PAE (16%) was observed when the circuit was biased (V_{EB} = -1.65 V and V_{CB} = 7.0 V) for optimum PAE, as shown in Fig. 8. The maximum PAE was achieved at a 2.2 dB gain compression point with a measured linear gain of 7.5 dB. The output power at the peak value of PAE is 21.1 dBm and saturated at 23.1 dBm.

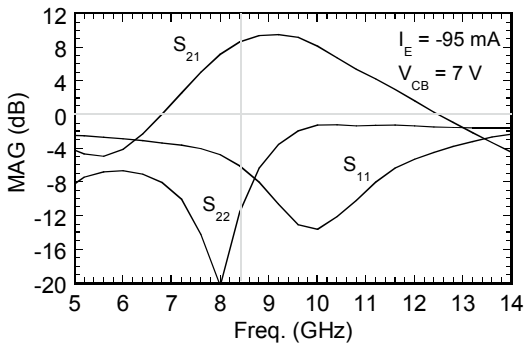

Fig. 6. Small-signal performance of SiGe/Si HBT MMIC power amplifier.

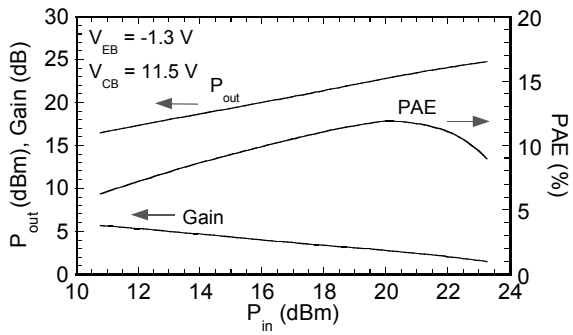

Fig. 7. Power performance of X-band MMIC power amplifier biased at V_{EB} = -1.3 V and V_{CB} = 11.5 V.

It has been found, in this study, that by reducing the resistive losses in the passive components, the power amplifier efficiency can be significantly increased. The simulated power performance of the same circuit with passive components of desired level of serial resistance and Q-factors (developed separately on an identical Si substrate) is shown in Fig. 9. A peak PAE of 25% can be realized with increased output power level (23.5 dBm) and associated power gain (5.3 dB). On the other hand, our recent study has shown that there is room to further improve the performance of the SiGe/Si power HBTs in terms of gain, output power and PAE [10]. As a result, higher performance power amplifies with SiGe-based HBTs and lumped passive on-chip components are achievable and these power amplifiers are currently being developed.

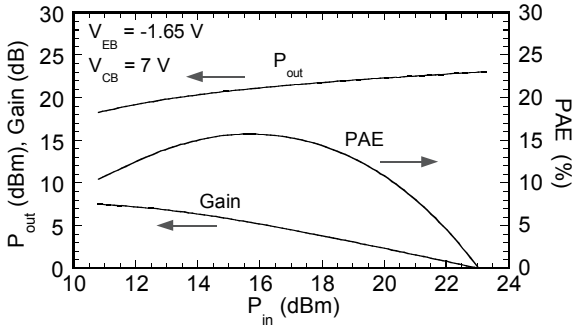

Fig. 8. Power performance of MMIC power amplifier biased at V_{EB} = -1.65 V and V_{CB} = 7.0 V.

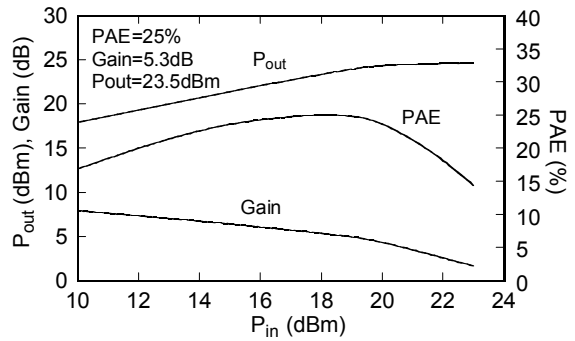

Fig. 9. Simulated power performance with high-Q spiral inductors. P_{out} = 23.5 dBm at peak PAE of of 25%. The power gain at peak PAE is 5.3 dB.

The demonstration of the first X-band Si-based MMIC power amplifier is an important step toward the system-on-a-chip solution for future communication applications and, currently, it shows the feasibility of integrating Si-based microwave power transistors with other passive components on a single chip. Based on this preliminary achievement, a highly integrated microwave transmitter based on Si, with reduced volume and weight, seems feasible. Due to the low cost of Si, the MMIC-type approach for this application also means a low cost for mass production.

IV. CONCLUSION

A single-stage X-band MMIC power amplifier incorporating a SiGe/Si HBT and lumped on-chip passive components has been demonstrated. The SiGe/Si power HBTs are characterized by an extrapolated f_{max} of 67 GHz. At 8.4 GHz, the power amplifier exhibits an output power of 22.9 dBm at peak PAE and a saturation output power of 24.8 dBm. It was found that the resistive loss in the passive components accounts for the major loss in the MMIC and improved processing techniques can potentially lead to 25% PAE, 23.5 dBm output power with concurrent 5.3 dB power gain from the same circuit.

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