A Stitching Technique for Expanding Large 3-D Multi-Layer Antenna Arrays in Ku-Band Using Small Array Units

David J. Chung[1], Swapan Bhattacharya[1], George Ponchak[2], and John Papapolymerou[1]
[1]Georgia Institute of Technology, School of Electrical and Computer Engineering, Atlanta, GA 30308
[2]NASA Glenn Research Center, Cleveland, OH 44135
Email: gth049a@mail.gatech.edu

Abstract

This paper presents an approach, where via technology is used to expand an antenna array by "stitching" two unit arrays. This method becomes useful as the processing capability becomes limited by the size of the antenna array. Using the bonding process of Liquid Crystal Polymer (LCP), a 3-D multi-layer 4x8 patch antenna array has been created and measured at 14 GHz. The results are compared to a single layer structure without vias. The measurement shows S11 of -19.1 dB at 13.9 GHz for the multilayer design with a via.

Introduction

As the demand for smaller devices grows, multilayer integration has become a key technology to optimize the compactness of a design. Using LCP, System On Package (SOP) level integration has been demonstrated [1], [2]. This approach takes advantage of the ease of multilayer stacking of LCP substrate through thermal compression bonding. The two different types of LCP, differentiated by the melting points, allow the bonding and stacking of a single substrate. The high melt melts at 300 ^{0}C while the low melt melts at 280 ^{0}C. In addition to these physical advantages, the low cost and superior RF characteristics of LCP at high frequencies make the substrate even more appealing for RF applications [3], [4].

One application that can benefit much from the multilayer design is arrayed antennas. Antenna arrays give the advantage of high directivity and gain, which are essential for military and space applications. For these applications, the size of the array can increase very quickly and multilayer antenna arrays help optimize the compactness. By separating the elements of the antenna array and possibly active components in the system to different layers, the density of the design can be maximized. Furthermore, trying to decrease the overall size in a single layer can give rise to coupling between the feeding elements and radiating elements. Again, the multilayer approach can help eliminate this problem by incorporating an embedded ground. Previous works have shown multilayer flexible antenna arrays with embedded ground, which also includes slots for the coupling between the feeding elements and radiating elements [5]-[7]. Yet, in another work, a phase shifter has been added into the feed network to make a compact reconfigurable antenna array [8]. With the near hermetic property of LCP, the bonded layers can protect the embedded circuitry as well. Though the multilayer design offers these advantages, the challenge remains for big arrays outside the fabrication capabilities.

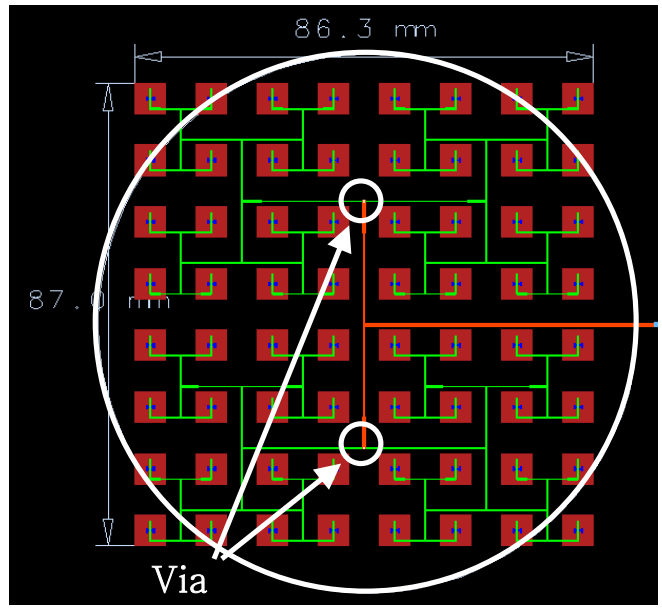


Fig.1. Two 4x8 antennas "stitched" together to form an 8x8 array. The circle denotes the fabrication size limit of 4 inches.

In this paper, via technology is used to overcome the processing limitation of size. The vias allow a connection between different layers, which ultimately connects unit arrays. A 4x8 antenna array has been chosen as the unit array because it is the maximum size that fits in the 4 inch wafer circle. By showing the possibilities of this "stitching" technique, the array can be expanded as far out as possible, limited only by the line and substrate loss.

Antenna Design

As shown in Fig.1, the 8x8 antenna array is larger than a 4 inch circle, the desired processing limit. It is possible to process bigger sample sizes, but at the cost of yield and non-uniformity across the sample. Also, with larger samples, the guaranteed minimum feature size becomes larger than desired and again, it may not be uniform. In addition, 4 inch wafers are popular for the development of high yield active RF circuits (Si or GaAs). In order to avoid these fabrication complications, a 4x8 antenna array is the unit array and "stitched" to create a larger 8x8 antenna array. The vias seen in the figure are connecting the probe line on the bottom to the embedded feed line.

Fig.2 shows both the layout of a 4x8 antenna array and the stacking of all the layers. The antenna uses approximately the half wave microstrip patches that are separated by 0.46λ . Two 4 mil LCP and two 2 mil LCP layers are bonded for a

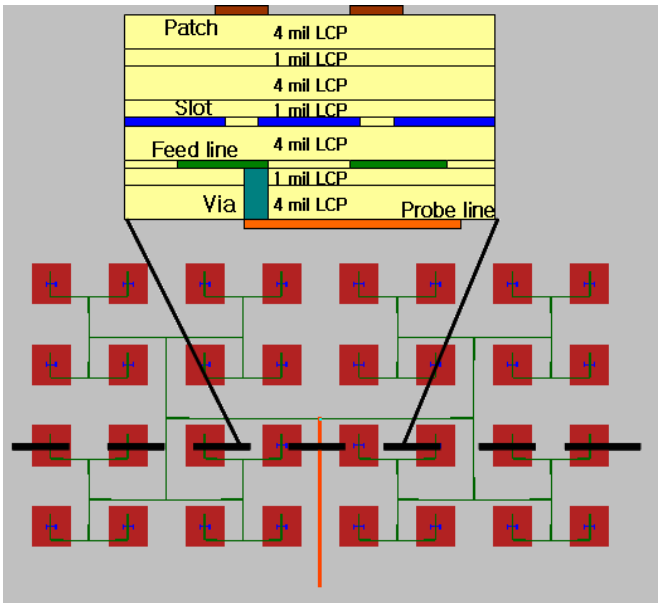


Fig. 2. A 4x8 unit array layout and the side view showing the stack up of multiple layers, 4 mil (high melt) and 1 mil (low melt) LCP. All metallization is Cu.

10 mil separation between the patch layer and slot layer. The slot layer provides coupling from the feed line layer to the patch layer, allowing simplification of the overall connection between the patch and feed line. In addition, the slot layer acts as the microstrip ground for all of the other layers and electrically isolating the top half from the bottom half. The feed line uses a symmetric corporate feeding network that eases the process of expanding the array, limited only by the conduction loss as the size increases. At each junction, an impedance transformer is used to effectively match the impedance of each output for the signal to split in half. At the bottom, there is the probe line layer where the measurement probe or SMA connector can be attached. Fig.2 shows clearly how the 250 µ m via is making the connection from the probe line layer to the feed line layer.

Fig.3 shows the simulation results of the corporate feed network in a single layer versus the multilayer network described above, which includes the via transition. Because the via adds parasitic capacitance and loss to the network, the overall response is slightly degraded. In general, this degradation is small enough so that the overall desired response at 14 GHz can still be observed.

Several different approaches were used to create the vias. One approach was using conductive silver epoxy to fill the vias. It is a convenient way but at high frequencies, the size of the vias becomes crucial as they introduce parasitic elements. Trying to manually fill a via-hole smaller than 500µ m also becomes a complication. Another consideration was taken with the design rules for industry standards, which is set to ensure good connections with high yield. Fig. 4 (a) shows a via created according to the design rules, and (b) shows a via just for a simple connection. The design rules for the industry

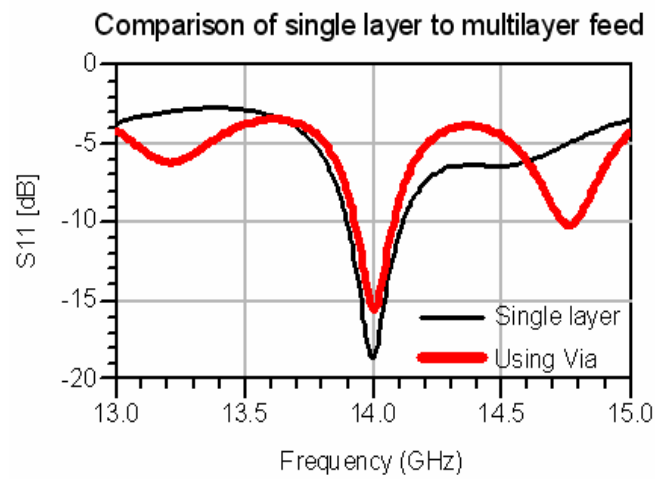
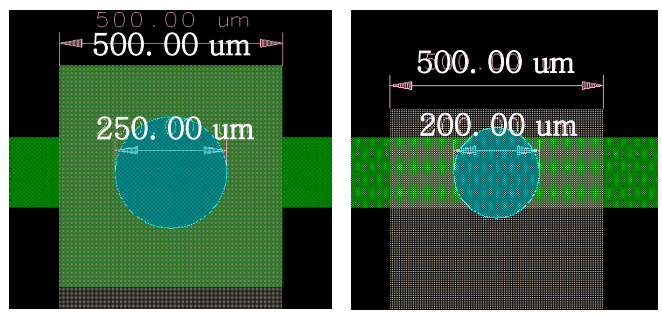


Fig.3 Comparison of the response of a 4x8 antenna array feed network in a single layer to a multilayer feed network including a via.



(a) (b)

Fig.4. Creating vias (a) 250µ m via complying to industry standard. (b) 200µ m via for a simple connection.

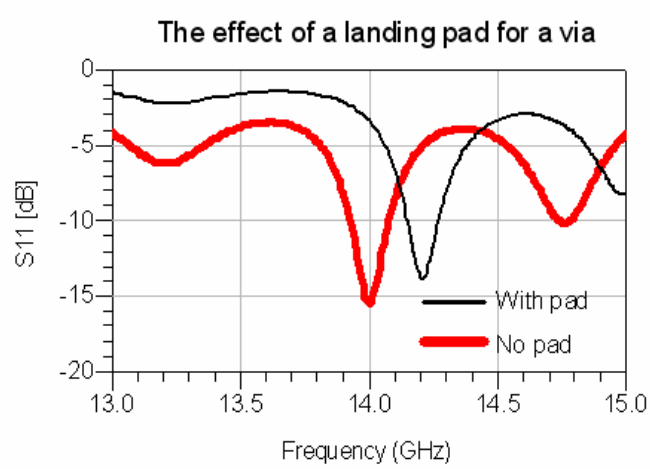


Fig.5. Comparison of the response with and without a 500µ m x 500µ m landing pad for a 250µ m via.

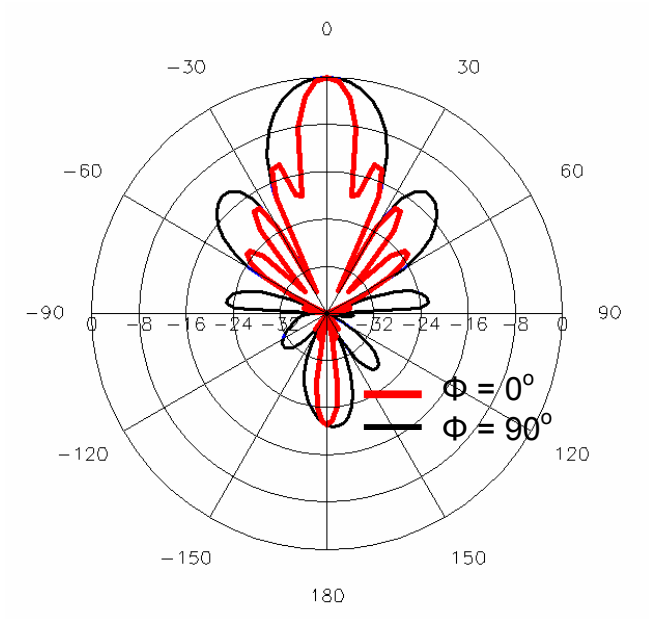


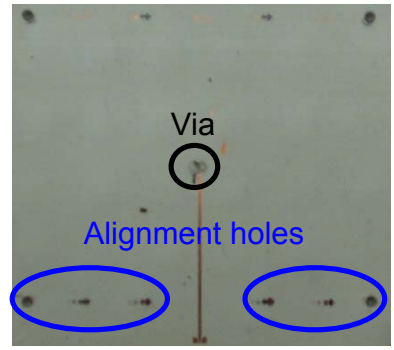
Fig. 6. Simulated E-field pattern of the 4x8 array with $\varphi = 0^o$ and $\varphi = 90^o$.

is to have a via hole size that is double that of the vertical length. Since there is 5 mil (≈ 125 μ m) LCP between the probe layer and feed layer, the via must be at least 250μ m. In addition, the via needs a large enough area around it, that is double the size of the via, to ensure good contact between the layers and compensate for the misalignment. Hence, a 500μ m x 500μ m pad is inserted in the feed layer and extra room is reserved in the probe layer. This extra pad in the feed layer and the extra area in the probe layer add parasitic capacitance and can throw off the impedance matching of the circuit. These parasitic effects can be seen in Fig.5, with a 0.2 GHz frequency shift for the resonance. Thus, with the addition of a landing pad, the feed network needs to be re-optimized to compensate for the parasitic effects introduced by the pad, in order to obtain the right response. For an initial result with a short turnaround time, the via has been made without a landing pad and sputtered copper has been used to fill the vias and create the contact between the layers. In addition, an area that is only 50μ m beyond the via has been given for the probe layer as seen in Fig.4 (b), which has been sufficient for a good contact.

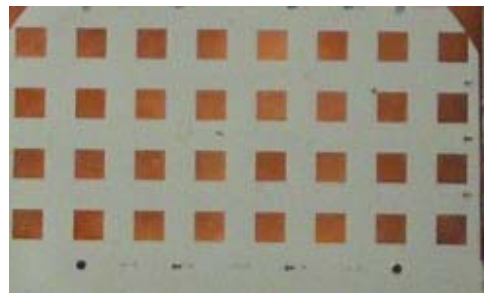
The simulated E-field pattern is shown in Fig. 6 for the 4x8 antenna array. The side lobe level is about 14 dB below the main beam for both cuts. It is clear that by having more elements along the $\varphi = 0^o$ axis, the beam is narrower and more directive. This is the reason for designing larger arrays especially for military and space applications.

Fabrication

All fabrication has been done at the Georgia Tech MiRC cleanroom facility. Using the 4 mil high melt LCP with 1/4 ounce double sided copper clad material, the copper is etched off or patterned as needed for different layers. CO2 laser is used to create the via and necessary alignment holes for



(a)



(b)

Fig. 7. Fabricated sample (a) probe layer side (b) patch layer side.

bonding. Because LCP is a flexible material, it is important to spend time to make the samples as flat as possible. Once all the layers are ready, except for the probe layer that will be sputtered, the sample is placed in an aluminum fixture and bonded with a Karl Suss Bonder. The bonder offers thermal compression bonding at a temperature in which only the low melt LCP melts. The process is optimized to have the low melt soften at an elevated temperature. Once the temperature is reached, then enough pressure is applied to break the molecular bonds of the low melt LCP and create new bonds with the high melt LCP while avoiding overflow. Once all the layers are bonded, the probe line layer is sputtered on, which will also fill the via, and then patterned using lithography process. The final sample is shown in Fig. 7 while the slot and feed lines are embedded in the design. The laser drilled alignment holes can be seen as well.

Many issues are present with processing a flexible material, in which the biggest difficulty is acquiring a good alignment throughout the fabrication process. Because the alignment holes are made with the laser, there is no guarantee that every single hole is going to be the exact same size. Also, for front and back patterning, the misalignment can be as bad as 50 μm so that an intuitive process must be taken to minimize these misalignments.

Measurements and Results

The fabricated antenna is tested with a vector network analyzer for the S11 measurements. A coaxial connector has been used to connect the sample and the input from the

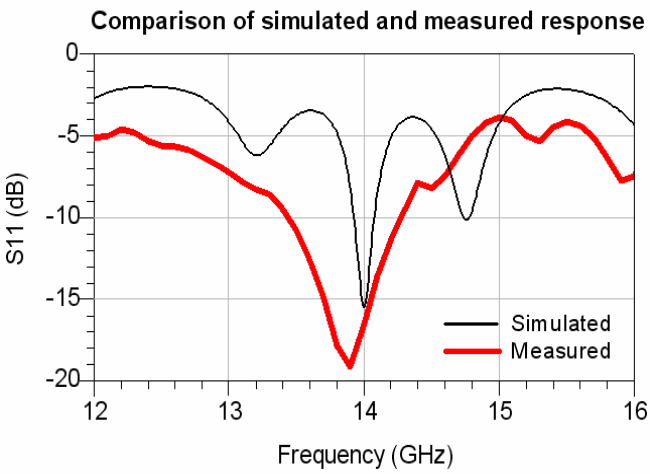


Fig. 8. Measured and simulated S11 response.

analyzer. The measurement result is shown in Fig.8 compared to the simulated measurements. The resonance is clear at 13.9 GHz with a S11 value of -19.1 dB. In order to verify the resonance is the actual radiation, a metal plate has been placed in the vicinity of the patch layer, covering all the patches, and we observed the resonance disappear. The overall loss is slightly higher than the simulated response which can be due to fabrication tolerances, such as over-etching and misalignment previously discussed, and the metal quality of the copper lines. In addition, since the calibration was done using a short, open, and load (SOL) calibration technique, this does not account for the connector loss and the transition loss expected to be at least 0.3 dB at 14 GHz. Another point in the figure is that the bandwidth is slightly larger than the simulated response. This is probably due to some additional loss in the overall antenna assembly.

Conclusions

The well known via process has been utilized for a new application of connecting two or more, smaller unit designs. As multilayer process brings many benefits to designs and applications, using the vias to connect unit designs or building blocks, can help overcome the processing limits. Smaller size samples, giving better processing yield, can be connected together to construct a larger design.

This paper presents one application in which the via process has been used for expanding the overall size beyond the fabrication limits. A multilayer 8x8 antenna array has been designed at 14 GHz using this "stitching" technique, and has been compared to the process without the via connection. The via introduces small parasitic effects that does not deteriorate the overall response much, proving the technique can be useful for expanding arrays beyond the simple unit array.

Acknowledgments

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